WHAT IS CLAIMED IS:

1. A method of forming a gate structure in an integrated circuit on a substrate, the method comprising the steps of:
forming a high k layer on the substrate,
forming a gate electrode layer on the high k layer,
patterning the gate electrode layer,
forming LDD regions using an ion implantation process, thereby creating damaged portions of the high k layer,
removing a first portion of the damaged portions of the high k layer, thereby defining a gate structure, and leaving remaining portions of the damaged portions of the high k layer,
forming sidewall spacers adjacent the gate structure,
forming source/drain regions using an ion implantation process, thereby further damaging the remaining portions of the damaged portions of the high k layer, and
removing the remaining portions of the damaged portions of the high k layer.

2. The method of claim 1, wherein the high k layer comprises hafnium dioxide.

3. The method of claim 1, wherein the high k layer comprises at least one of HfSiON, ZrO_2, HfON, La_2O3, CeO_2, Na_2O_3, Sm_2O_3, Eu_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3, Tm_2O_3, Yb_2O_3, Lu_2O_3.

4. The method of claim 1, wherein the LDD implanted species comprises arsenic.

5. The method of claim 1, wherein the LDD ion implantation is conducted at a dopant level of about $6(10)^{13}$ atoms per square centimeter.

6. The method of claim 1, wherein the LDD ion implantation is conducted at an energy of about eighty thousand electron volts.

7. The method of claim 1, wherein the first portion of the damaged portions of the high k layer is removed using a solution of hydrofluoric acid.

8. The method of claim 1, wherein the source/drain implanted species comprises arsenic.

9. The method of claim 1, wherein the source/drain ion implantation is conducted at a dopant level of about $3(10)^{15}$ atoms per square centimeter.

10. The method of claim 1, wherein the source/drain ion implantation is conducted at an energy of about forty thousand electron volts.

11. The method of claim 1, wherein the remaining portions of the damaged portions of the high k layer are removed using a solution of hydrofluoric acid.

12. The method of claim 1, further comprising the step of forming a base interface layer on the substrate prior to the step of forming the high k layer.

13. The method of claim 1, wherein the high k layer is formed using at least one of a metallorganic chemical vapor deposition process, an atomic layer deposition process, and a physical vapor deposition process.

14. The method of claim 1, wherein the gate electrode layer is formed of at least one of polycrystalline silicon and polycrystalline germanium.

15. A method of forming a gate structure in an integrated circuit on a substrate, the method comprising the steps of:

forming a base interface layer on the substrate,

forming a high k layer on the base interface layer,

forming a gate electrode layer of polycrystalline silicon on the high k layer,

patterning the gate electrode layer,

forming LDD regions using an ion implantation process, thereby creating damaged portions of the high k layer,

removing a first portion of the damaged portions of the high k layer, thereby defining a gate structure, and leaving remaining portions of the damaged portions of the high k layer,

forming sidewall spacers adjacent the gate structure,

forming source/drain regions using an ion implantation process, thereby further damaging the remaining portions of the damaged portions of the high k layer, and

removing the remaining portions of the damaged portions of the high k layer.

16. The method of claim 15, wherein the high k layer comprises hafnium dioxide.

17. The method of claim 15, wherein the high k layer comprises at least one of HfSiON, ZrO_2, HfON, La_2O3, CeO_2, Na_2O_3, Sm_2O_3, Eu_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3, Tm_2O_3, Yb_2O_3, Lu_2O_3.

18. A method of forming a gate structure in an integrated circuit on a substrate, the method comprising the steps of:

forming a base interface layer on the substrate,

forming a high k layer on the base interface layer,

forming a gate electrode layer on the high k layer,

patterning the gate electrode layer,

forming LDD regions using an ion implantation process, thereby creating damaged portions of the high k layer,

removing a first portion of the damaged portions of the high k layer, thereby defining a gate structure, and leaving remaining portions of the damaged portions of the high k layer,

removing a first portion of the base interface layer underlying the first portion of the damaged portions of the high k layer, and leaving remaining portions of the base interface layer underlying the remaining portions of the damaged portions of the high k layer,

forming sidewall spacers adjacent the gate structure,

forming source/drain regions using an ion implantation process, thereby further damaging the remaining portions of the damaged portions of the high k layer,

removing the remaining portions of the damaged portions of the high k layer, and

removing the remaining portions of the base interface layer.

19. The method of claim 18, wherein the high k layer comprises hafnium dioxide.

20. The method of claim 18, wherein the high k layer comprises at least one of HfSiON, ZrO_2, HfON, La_2O3, CeO_2, Na_2O_3, Sm_2O_3, Eu_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3, Tm_2O_3, Yb_2O_3, Lu_2O_3.